International Test Conference
2013 Advance Program

Test Week
September 8-15, 2013

Conference & Exhibition
September 10-12, 2013

Disneyland Hotel, Anaheim,
California, USA
It is our privilege to welcome you to the 44th IEEE International Test Conference (ITC) sponsored by the IEEE Computer Society and the Philadelphia Section. This year the conference returns to the same venue as last year, the Disneyland Resort Hotel in Anaheim, California, during the week of September 9, 2013.

If you are a regular attendee to ITC, then you already know that ITC is the world’s premier conference dedicated to electronics test technology for devices, boards and systems—covering the complete cycle from design verification, test, diagnosis, failure analysis, customer quality/reliability and back to process and design improvement. It’s also a great opportunity to meet your professional colleagues, make new friends and catch up with old friends.

If you have never attended ITC then you will soon discover the wealth of learning and networking opportunities in the field of test, which ITC has become famous for. This includes two days of half-day tutorials taught by the leading experts in their respective fields, three keynote speeches from leading industrialists, a series of Advanced Industrial Practices (AIP) sessions and an embedded workshop for attendees to learn the latest methods and techniques used by industry leaders. There will be numerous opportunities to meet and greet others in the profession in a fun-filled atmosphere through the various social functions. The Disneyland Resort provides ample opportunities for networking before, during and after the conference. With the Downtown Disney venue only steps away from the host hotel, there will be plenty of opportunities for corporate events and late-night socializing. We also encourage you to take advantage of the advance-purchase discounted theme park tickets, which are available to attendees and exhibitors. Please see the hotel reservation link to access this ticket opportunity.

The 2013 technical program will have 46 paper presentations covering various topic areas, five panel sessions and a poster session. Three specialized workshops will also be collated with the conference on hot topics such as debug and validation, test of 3-D ICs, and more.

There will also be several open technical activities meetings held throughout the conference. These meetings include standards working groups as well as others.

As always, and what sets ITC apart, is the broad and diverse exhibitor floor comprised of EDA, hardware and test solutions providers covering almost any test need. The exhibit floor is where you can see theory put into practice. Participating in demos and talking to the exhibitors is an integral part of the ITC experience, and one that lets you compare competing test solutions quickly and efficiently. The exhibit floor area will also be the site for the poster session as well as the Corporate Forum that will highlight new and exciting developments in test equipment, services, tools and methodologies. Returning in 2013 is the Exhibit Hall ITC Passport Program. Stamped passports can be turned in for an opportunity to win prizes.

On behalf of the International Test Conference 2013 steering committee, program committee and all the dedicated volunteers who are key to making the program complete, we look forward to welcoming you to this year’s exciting technical program and exhibits.

See you in September!

Gordon Roberts
General Chair

Rob Aitken
Program Chair

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Silver

Bronze

Gordon Roberts
General Chair

Rob Aitken
Program Chair
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**SUNDAY, SEPTEMBER 8 – HALF-DAY TUTORIALS**

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<th>Time</th>
<th>Tutorial 1</th>
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<th>Tutorial 3</th>
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<tbody>
<tr>
<td>8:30 a.m. –</td>
<td>Testing of TSV-based 2.5D- and 3D-Stacked</td>
<td>Mixed-Signal DFT and BIST: Trends,</td>
<td>Reconciling the Dichotomy Between Test</td>
</tr>
<tr>
<td>12:00 p.m.</td>
<td>ICs—Basic</td>
<td>Principles and Solutions</td>
<td>and Security</td>
</tr>
<tr>
<td>1:00 p.m. –</td>
<td>Testing of TSV-based 2.5D- and 3D-Stacked</td>
<td>Clock and Serial Data Communication</td>
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</tr>
<tr>
<td>4:30 p.m.</td>
<td>ICs—Advanced</td>
<td>Channel Testing</td>
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**MONDAY, SEPTEMBER 9 – HALF-DAY TUTORIALS**

<table>
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<th>Time</th>
<th>Tutorial 7</th>
<th>Tutorial 8</th>
<th>Tutorial 9</th>
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<tbody>
<tr>
<td>8:30 a.m. –</td>
<td>Delay Test: Concepts, Theory and Recent</td>
<td>Hierarchical Test: Trends, Challenges</td>
<td>Statistical and Adaptive</td>
</tr>
<tr>
<td>12:00 p.m.</td>
<td>Trends</td>
<td>and Solutions</td>
<td>Testing</td>
</tr>
<tr>
<td>1:00 p.m. –</td>
<td>Testing Low-Power Integrated Circuits</td>
<td>Tutorial 13</td>
<td>Tutorial 15</td>
</tr>
<tr>
<td>4:30 p.m.</td>
<td></td>
<td>Advanced Memory BIST and Repair in</td>
<td>Collaborative Yield Learning</td>
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<td>Nanometer Era</td>
<td>in Advanced Technologies</td>
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<td></td>
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<td>System Level Test and Diagnosis</td>
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**MONDAY, SEPTEMBER 9 – SPECIAL PANEL**

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<tr>
<th>Time</th>
<th>Panel 1</th>
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<tr>
<td>4:30 p.m. –</td>
<td>The Future of Test Automation - Where</td>
</tr>
<tr>
<td>6:00 p.m.</td>
<td>Should We Place Our Bets?</td>
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<td>7:00 p.m.</td>
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**MONDAY, SEPTEMBER 9 – POST-PANEL RECEPTION**

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<tr>
<th>Time</th>
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<td>7:30 p.m.</td>
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**TUESDAY, SEPTEMBER 10 – TECHNICAL SESSIONS**

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<tr>
<th>Time</th>
<th>Plenary – Keynote Address Challenges in Mobile Devices: Process, Design and Manufacturing</th>
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<tr>
<td>9:00 a.m. –</td>
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<tr>
<td>10:30 a.m.</td>
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<tr>
<td>11:00 a.m.</td>
<td></td>
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<tr>
<td>12:00 p.m.</td>
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</tr>
<tr>
<td>2:00 p.m. –</td>
<td>Session 1 ATE Solutions—All the Way to Light Speed</td>
</tr>
<tr>
<td>3:30 p.m.</td>
<td>Session 2 Finding the Gems in the Test Data Mine</td>
</tr>
<tr>
<td>4:00 p.m. –</td>
<td>Session 3 2.5D/3D -IC DFT</td>
</tr>
<tr>
<td>5:30 p.m.</td>
<td>Session 4 Scan Compression for Large Designs</td>
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<td>Session 5 DFT and Security</td>
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<td>Session 6 Where Are the Waldos of DFT?</td>
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**TUESDAY, SEPTEMBER 10 – ITC GRAND RECEPTION**

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<th>Advanced Industrial Practices 1</th>
<th>Advanced Industrial Practices 2</th>
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<tr>
<td>8:30 a.m. – 10:00 a.m.</td>
<td>3-D/TSV Testing</td>
<td>Post-Silicon Validation and Debug</td>
<td>On-Chip Monitoring and Sensing</td>
<td>Advanced Measurement Techniques</td>
</tr>
<tr>
<td>9:30 a.m. – 4:30 p.m.</td>
<td>Exhibits</td>
<td>Advanced Industrial Practices 3</td>
<td>Challenges of New Technologies</td>
<td></td>
</tr>
<tr>
<td>10:00 a.m. – 3:00 p.m.</td>
<td>Corporate Forum</td>
<td>Advanced Industrial Practices 4</td>
<td>Low-Cost Test with High-End Testers</td>
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</tr>
<tr>
<td>10:30 a.m. – 12:00 p.m.</td>
<td>Session 8 Managing Tests for Complex SOCs</td>
<td></td>
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<td>Panel 3 What Is the Future for 3-D?</td>
</tr>
<tr>
<td>12:00 p.m. – 2:00 p.m.</td>
<td>Poster Session - Lunch</td>
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<tr>
<td>2:00 p.m. – 4:00 p.m.</td>
<td>Session 9 Protocols/Methodologies for Test Time Reduction</td>
<td>Session 10 Advances in Test Generation</td>
<td>Lecture 3 Hardware Security and Trust</td>
<td>Session 11 Board Test Methods</td>
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<tr>
<td>4:30 p.m. – 5:30 p.m.</td>
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<td>Ph.D. Thesis Competition Forum</td>
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**Keynote Address**: Compute Continuum and the Nonlinear Validation Challenge

### THURSDAY, SEPTEMBER 12 – TECHNICAL SESSIONS

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<th>Session 13 Monitoring and Mitigating Aging</th>
<th>Session 14 Reliability and Test of FPGAs and Memories</th>
<th>Embedded Workshop DATA Workshop</th>
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<tr>
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<tr>
<td>9:30 a.m. – 1:00 p.m.</td>
<td>Exhibits</td>
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<tr>
<td>11:00 a.m. – 12:00 p.m.</td>
<td>Keynote Address: Efficient Resilience in Future Systems: Design and Modeling Challenges</td>
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<tr>
<td>12:00 p.m. – 1:00 p.m.</td>
<td>Lunch</td>
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<tr>
<td>1:00 p.m. – 2:30 p.m.</td>
<td>Lecture 4 Test Methods for HF Signals</td>
<td>Session 14 Reliability and Test of FPGAs and Memories</td>
<td>Embedded Workshop DATA Workshop</td>
<td>Session 15 DFT advances</td>
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<tr>
<td>3:00 p.m. – 4:30 p.m.</td>
<td>Panel 4 Challenges of SerDes and DDR Defect Testing and AC Spec Measurements</td>
<td>Adv. Industrial Practices 6 Experiences with System-level Test</td>
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### THURSDAY, SEPTEMBER 12 – TWO-DAY WORKSHOPS

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<td>7:30 p.m. – 9:30 p.m.</td>
<td>Workshop Reception</td>
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### FRIDAY, SEPTEMBER 13 – TWO-DAY WORKSHOPS

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<th>Embedded Workshop DATA Workshop</th>
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TTTC TEST TECHNOLOGY EDUCATION PROGRAM (TTEP) 2013

The Tutorials & Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes a comprehensive set of Test Technology Tutorials to be held in conjunction with several TTTC-sponsored technical meetings worldwide. The mission of the Test Technology Educational Program (TTEP) is to serve test and design professionals by offering fundamental education and expert knowledge in state-of-the-art test technology topics. TTEP offers tutorial participants the opportunity to earn official certification from IEEE Computer Society TTTC. Each half-day tutorial corresponds to two TTEP units. Upon completion of 16 TTEP units, official recognition in the form of an IEEE TTTC Test Technology Certificate will be presented to the participant. For further information regarding TTEP, please visit http://tab.computer.org/tttc/ttg/ttep/

At ITC 2013, TTTC/TTEP is pleased to present 13 half-day tutorials on topics of current interest to test professionals and researchers. All tutorials qualify for credit towards IEEE TTTC certification under the TTEP program. Six tutorials are held on Sunday, September 8. Ten tutorials will be held on Monday, September 9. Each tutorial requires a separate registration fee (see registration page or http://www.itctestweek.org for further information). Admission for onsite registrants is subject to availability. Tutorial attendees receive study material and coffee breaks. Lunch will be provided for those attending consecutive tutorials on the same day, e.g., Tutorial 1 and Tutorial 4. The study material includes a hardcopy of the presentation and bibliographical material. Tutorial registration, coffee and pastries are available at 7:30 a.m. on Sunday and Monday.

Sunday  8:30 a.m. – 12:00 p.m.

TUTORIAL 1
Testing of TSV-based 2.5D- and 3D-Stacked ICs—Basic

Presenters E.J. Marinissen, K. Chakrabarty

Description Stacked ICs with vertical interconnect containing fine-pitch microbumps and through-silicon vias (TSVs) are a hot-topic in design and manufacturing communities. These 2.5D- and 3D-SICs hold the promise of heterogeneous integration, inter-die connections with increased performance at lower power dissipation, and increased yield and hence decreased product cost. However, testing for manufacturing defects remains an obstacle and potential showstopper before 3D-SICs can become a reality. There are concerns about the cost or, even worse, feasibility of testing such TSV-based 3D chips.

In this basic tutorial, we present key concepts in 3D technology, terminology, and benefits. We discuss design and test challenges and emerging solutions for 2.5D- and 3D-SICs. Topics to be covered include an overview of 3D integration and trendsetting products such as a 2.5D-FPGA and 3D-stacked memory chips, test flows and test content for 3D chips, advances in wafer probing reported by probe companies, modular testing and design-for-test architectures, and ongoing IEEE P1838 standardization efforts for test access.

TUTORIAL 2
Mixed-Signal DFT and BIST: Trends, Principles and Solutions

Presenter S. Sunter

Description We start by briefly looking at trends in process, design, and analog/mixed-signal testing, then in more detail at trends in ad hoc design-for-test (DFT) and analog defect simulation. We then review standardized DFT suitable for mixed-signal circuits, including IEEE 1149.1, .4, .6, .8, and 1687. The trend analysis concludes with an analysis of BIST techniques, especially for ADC/DAC, but also for PLL, SerDes, DDR, and miscellaneous analogue. Next, seven essential principles of practical analog BIST are discussed, ranging from testing the BIST itself, and adding for precision, to subtracting for accuracy, and generating a digital result. Lastly, we discuss the most practical techniques to use in new DFT and BIST circuitry, ranging from the classic analog test bus, to mostly digital oversampling and undersampling circuits that improve measurement range, resolution, and reusability, to ultimately optimize quality and cost of test.

TUTORIAL 3
Reconciling the Dichotomy Between Test and Security

Presenter R. Karri, O. Sinanoglu

Description Hardware security is an important optimization objective for designs (similar to power, performance, reliability and testability). We will highlight why hardware security and trust are as important as these other objectives from the economics of security, IP protection and counterfeiting perspectives. We will then describe the simple gotchas when traditional DFT and validation techniques are used (scan chains, JTAG, SOC test, assertion based validation). Next, we will outline how traditional DFT techniques can be used to improve hardware security and trust. Finally, we will present “design-for-trust” approaches that can provide testability without compromising security and trust.
For the most part, these methods are based on jitter decomposition techniques, i.e., probabilistic methods that describe the underlying structure of the randomness present with the asynchronous signal. Commonly used jitter terms such as random, deterministic and total jitter abbreviated to RJ, DJ and TJ metrics will be described using the concept of a Gaussian mixture model. This tutorial will conclude with a discussion of several DSP-based test techniques used to quantify jitter transmission from the system input to its output. This includes a discussion about jitter transfer function test and a jitter tolerance test. Some discussion of DFT methods for jitter extraction will also be given. These will be presented from a time-domain signal processing perspective.
Monday 8:30 a.m. – 12:00 p.m.

**TUTORIAL 7**  
Delay Test: Concepts, Theory and Recent Trends  
Presenters S. Natarajan, A. Sinha  

**Description**  
This tutorial covers fundamental concepts, recent developments and industry practices on validating and testing integrated circuits for speed failures. The intended audience is a combination of semiconductor industry practitioners, EDA technologists, and researchers in digital test. The tutorial starts with a discussion on defects and design marginalities that induce a circuit to fail at its rated speed while passing at a lower speed. This is followed by fault models and fault sensitization conditions, for classical faults such as transition and path delay, and for marginalities such as crosstalk, voltage droop, multiple-input switching and charge-sharing. Subsequently, concepts in test generation and fault simulation for delay faults are discussed. Recent advances in delay-test-specific DFT techniques, timing-aware metrics for test quality, and techniques to improve defective parts per million (DPPM) and reduce yield loss, are described. Finally, industry case studies that apply delay test concepts in postsilicon validation, speed binning and in-field reliability are discussed.

**TUTORIAL 8**  
Hierarchical Test: Trends, Challenges and Solutions  
Presenters A. Cron, Y. Zorian  

**Description**  
Hierarchical design has come a long way in a very short time. The use of multilevel hierarchical test methodologies is, therefore, ramping up. Design teams use these architectures to handle the explosion in design size, liberal use of 3rd-party IPs, and the general use of multi-level hierarchical design (core, block, sub-chip, SOC) methodologies across geographically dispersed corporations and their design partners. To support these types of designs with appropriate DFT, design teams leverage IEEE standards-based methodologies to implement test in a hierarchical manner, across heterogeneous cores types (memories, logic, AMS, interface IP, and legacy cores). These hierarchical DFT design styles support DFT closure, power reductions during test, isolated debug and diagnosis, pattern porting, capacity improvements, and uniform and ubiquitous access. Using IEEE test standards such as 1149.1 and 1500 promote benefits such as these. CTL and STIL support these methodologies. The future P1687 is meant to allow instrumentation access, supported by test portability throughout the device life cycle. This tutorial covers these trends, design styles and methodologies, and how they are facilitated by IEEE test standards.

**TUTORIAL 9**  
Statistical and Adaptive Testing  
Presenter A. Singh  

**Description**  
Integrated circuits have traditionally all been tested identically in the manufacturing flow with little sharing of test results between the different test insertions. However, as the detection of subtle manufacturing flaws becomes ever more challenging and expensive in aggressively scaled nanometer technologies, innovative new statistical screening methods are being developed that attempt to improve test effectiveness and optimize test costs by subjecting “suspect” parts to more extensive testing, and also adaptively bring in additional tests that target the suspected failure modes. Adaptive test methods also support the dynamic reordering of test to achieve early failure detection resulting in significant savings in test application time. This tutorial presents an overview of these emerging test methodologies, and illustrates their effectiveness with results from a number of published experimental studies on volume production digital and analog circuits. Commercial tools offered by some of the new companies that have emerged in the “adaptive test” space will also be discussed.

Note: Tutorials 10 and 11 were canceled.
Monday 1:00 p.m. – 4:30 p.m.

**TUTORIAL 12**

**Testing Low-Power Integrated Circuits: Challenges, Solutions and Industry Practices**

**Presenters** S. Ravi, V. Chikermane, K. Chakravadhanula

**Description** The push for portable, battery-operated, and “cool-and-green” electronics has elevated power consumption as the defining metric of integrated circuit (IC) design. Testing ICs built for such applications requires judicious consideration of test power implications on various aspects of the design cycle (e.g., packaging and power grid design), test engineering (multi-site ATE power supply limitations and board design), power-aware test planning (DFT and ATPG), and developing the enabling EDA tool infrastructure (SW for estimation, reduction and low-power test generation). Physically-aware low-power test techniques are also becoming important for accuracy and hot-spot minimization, especially for designs at 22 nm and below. Furthermore, with power optimization and power management techniques becoming “de-facto” in almost all 45-nm and lower chips, systematic testing of these structures and the device in the presence of these structures becomes mandatory. This tutorial is intended to provide an overview of low-power IC testing covering (a) dimensions of power-aware testing, (b) methods for test power analysis and signoff, (c) techniques for controlling test power consumption and (d) test of power managed designs. Case studies illustrating industrial design deployment practices and existing EDA vendor support will also be outlined.

Moreover, with the adoption of FinFET technologies, these advanced solutions are extended to cover new FinFET-specific defects. This tutorial, besides addressing these defect detection topics, will cover an end-to-end BIST and repair architecture to handle tens of thousands of embedded memory instances in today’s SOC, while taking into account power management constraints, functional timing implications, test scheduling flexibility, and area minimization options. With the proliferation of high-density packaging technologies, such as 2.5D and 3D-ICs, this tutorial will also cover testing and diagnosis external memory dies and interconnects, via an advanced BIST engine residing in the neighboring SOC die, in same high-density package. This tutorial will also address post-silicon analysis and yield optimization trade-offs using volume diagnostic, failure coordinate calculation, defect classification, reconfiguration and repair.

**TUTORIAL 14**

**Data Mining In Test and Verification—Principles and Practices**

**Presenters** L-C. Wang, M. Abadir

**Description** This tutorial teaches the principles of various data mining approaches and their respective learning techniques. The approaches include classification, regression, transformation, feature ranking, clustering, novelty detection, rule learning and similarity search. We will illustrate the working principles of various learning techniques such as tree learning, random forest, neural network, support vector machine, Gaussian process, rule learning, etc. We will discuss application examples to illustrate how various learning approaches can be applied in test and verification. The experience of developing a practical data mining flow will be explained. We will show how data mining in practice implements an iterative knowledge discovery process. Promises of this knowledge discovery paradigm will be demonstrated through positive results based on several industrial application settings.

**TUTORIAL 15**

**Collaborative Yield Learning in Advanced Technologies**

**Presenter** R. Madge

**Description** Yield has become the defining metric for success and failure for semiconductor manufacturing at leading-edge technologies. The yield challenge has largely been driven the confluence of the design complexity and the advanced process and packaging technologies/materials. In addition, the factory (Fab) environment and the equipment toolset have also become significant contributors to the yield equation. The solution requires a strong collaborative teamwork approach involving designer, customer, equipment provider and the factory engineering and operations teams to ensure first-time yield success, product quality and profitability.

**TUTORIAL 16**

**System-level Test and Diagnosis**

**Presenter** W. Eklow, K. Chakraborty

**Description** As components continue to scale with Moore’s Law, complexity scales as well. Given that a system is comprised of a hierarchy of subsystems, where components are at the bottom of the hierarchy, one could claim that at a system-level scaling is exponential to Moore’s Law. A “system” can be anything that is in between an iPhone and IBM’s Watson. While these two “systems” seem quite diverse, there are plenty of similarities from a test perspective. This tutorial will begin with a description of what exactly is a system, and what are the elements that comprise a system (including software). We will talk about the hierarchical architecture of a system and the test process around that hierarchy. The majority of the tutorial will focus on testing and diagnosis at the system level (both functional and application based testing). This will include both online and offline testing, as well as validation testing, production testing and reliability testing. The tutorial will look at both traditional and innovative test techniques.
Visit the international exhibition that includes the latest high-technology test, design and service products.

Exhibits hours: Tuesday 10:30 a.m. – 5:30 p.m. 
Wednesday 9:30 a.m. – 4:30 p.m., Thursday 9:30 a.m. – 1:00 p.m.

FREE ADMISSION TO EXHIBITS

ITC is offering free exhibits-only registration to visit the exhibit hall during all exhibit hours. Onsite registration for this special opportunity begins on Tuesday at the ITC registration area in the Disneyland Hotel Conference Center. Lunch is not included with free admission.

Fill in your Exhibit Hall Passport for Prizes.

All registered attendees will receive a passport within their conference tote. Get your passport stamped Tuesday and Wednesday while visiting exhibitor booths and at least one Corporate Forum session. Drop your completed passport into the collection box located in the exhibit hall, and be eligible for the drawing at 4:00 p.m. on Wednesday in the exhibit hall. You need not be present at the time of drawing to win.

Prizes will consist of "Disney Dollars". Please see the full instructions included with your passport for details.
Aehr Test Systems
Aemulus Corporation Berhad
Alliance ATE Consulting Group, Inc.
Anora LLC
Aries Electronics
ASSET InterTech, Inc.
Atrenta, Inc.
Checkpoint Technologies, LLC
Chroma ATE, Inc.
CMR Summit Technologies
Cohu SEG
DCG Systems
DeFacTo Technologies
Evaluation Engineering
Evans Analytical Group (EAG)
Everett Charles Technologies
Exatron
Finley Design Services, Inc.
GOEPel Electronics LLC
Gorilla Circuits
High Connection Density
Integrated Semiconductor Solutions, Inc.
Integrated Test Corporation
Ironwood Electronics
ISC Technology Co. Ltd
JTAG Technologies
Lynxemi Pte Ltd
Marvin Test Solutions
Maxxmum, Inc.
Mechanical Devices
Mentor Graphics Corporation
Micro Control Company
Modus Test LLC
MPC Design Technologies, Inc.
Multitest
OptimalTest
PDF Solutions, Inc.
Omron Corporation
Qualtera
R&D Circuits
Ridgetop Group
Roos Instruments, Inc.
Salland Engineering
SEMICAPS Pte Ltd
Sensata Technologies
SL Power Electronics
SPEA America
Synopsys, Inc.
SynTest Technologies, Inc.
TDK-Lambda Americas
Teledyne Relays
Teradyne Global Services
Transcend Technologies LLC
TSSI
TTTC
Vermont Microdrilling
WinterLogic
XJTAG
Yamaichi Electronics USA, Inc.

* As of publication date.
Plenary & Keynote Address

Tuesday 9:00 a.m. – 10:30 a.m.

Opening Remarks
Gordon Roberts, ITC General Chair

ITC Paper Awards Presentation
Tim Cheng, ITC 2012 Program Chair

Keynote Address
Challenges in Mobile Devices: Process, Design and Manufacturing

Kwang-Hyun Kim, Executive Vice-President Samsung Electronics

The requirements for the recent mobile devices are significantly different from those for the conventional PC-oriented devices in many aspects: power consumption, performance and production ramp-up speed. These unique requirements have created many challenges in process technology, design, and manufacturing. Mobile devices are battery-sensitive, but still need the horsepower to run performance-hungry applications. We need a very tight DTCO (Design and Technology Co-Optimization), and a steep production ramp with high yield. Samsung Electronics has been focusing on the development and manufacturing of mobile devices for many years. The unique challenges associated with mobile devices will be addressed in the talk, along with our experience in overcoming them.

About the speaker: Kwang-Hyun Kim is Executive Vice-President and Head of foundry business in the System LSI Division of Samsung Electronics. He spent several years in Samsung’s R&D division focusing on library and IP development, and network and communication SOC development. He has held several leadership positions in the System LSI Division of Samsung Electronics including the Head of sales and marketing (2006-2010), and his current position as the Head of foundry business (2011-). Dr. Kim received the BS degree in Electronics Engineering from Sogang University in South Korea, and the MS and Ph.D. degrees in Electrical Engineering from Virginia Tech., USA.
Wednesday  4:30 p.m. – 5:30 p.m.

Compute Continuum and the Nonlinear Validation Challenge

John D. Barton, Vice-President, Platform Engineering Group, Intel Corporation

Intel architecture scales from Exa-scale computing to hand-held and deeply embedded devices. A consistent architecture spanning many product domains brings benefits to silicon and product developers. But it also creates a validation challenge that is nonlinear in nature due to the differences in product complexity, use cases, and user expectations. In this talk, John will address how Intel views the reliability/resilience of large scale systems, how we test for user experience that might help users decide what is good for them, how we attempt to balance all the conflicting validation requirements in today’s rapidly evolving landscape spanning consumption devices with short life spans to enterprise applications with very high uptime and reliability expectations. In addition, he will comment on the developments in formal methods and their applicability to large-scale commercial validation/verification efforts.

Thursday  11:00 a.m. – 12:00 p.m.

Efficient Resilience in Future Systems: Design and Modeling Challenges

Pradip Bose, Manager, Department of Power- and Reliability-Aware Microarchitectures. IBM Thomas J. Watson Research Center

The cost of maintaining current levels of hardware reliability appears to be unaffordable in the post-22 nm late CMOS design era. In the first part of this talk, we will examine the reasons behind such a projection, based on the modeled trends in technology, circuits and microarchitecture. Then, in the second part, we will present a vision of cross-layer resilience optimization, which forms the basis of an IBM-led project sponsored by DARPA under its PERFECT program. The goal is to demonstrate through parameterized, cross-layer modeling that such an approach can help provide cost- and energy-efficient resilience in a class of future embedded systems of interest to DARPA, U.S. Department of Defense and also to the general IT appliance industry. The modeling framework is targeted to be flexible enough that customized trade-off analyses are expected to be of value to other R&D efforts geared toward high-end server, mainframe, cloud and large-scale supercomputing market segments as well.

About the speaker Pradip Bose is with IBM, Yorktown Heights, NY, USA, where he manages the Department of Power- and Reliability-Aware Microarchitectures.

He has been involved in the design and pre-silicon modeling of virtually all IBM POWER-series microprocessors, since the pioneering POWER1 (RS/6000) machine, which started as the Cheetah/America superscalar RISC project at IBM Research. His current research interests are in embedded and high-performance computers, power-efficient, reliable microprocessor architectures, pre-silicon modeling and validation. Pradip holds MS and Ph.D. degrees from University of Illinois at Urbana-Champaign. His B.Tech (Hons.) degree was from Indian Institute of Technology Kharagpur in India. He has won numerous awards and honors from IBM—including sixteen Invention Plateau awards, several Outstanding Innovation Awards, Technical Achievement Awards and Research Division Awards. He also holds the title of IBM Master Inventor and is a member of IBM’s Academy of Technology. Dr. Bose served as the Editor-in-Chief of IEEE Micro from 2003-2006 and is the current Chairperson of ACM SIGMICRO. He is a Fellow of the IEEE.
Tuesday

2:00 p.m. – 3:30 p.m.

SESSION 1
ATE Solutions—All the Way to Light Speed
Z. Conors, Cisco Systems (Chair)

1.1 30-Gb/s Optical and Electrical Test Solution for High-Volume Testing
D. Watanabe, A. Ono, T. Okayasu, Advantest; S. Masuda, H. Haru, T. Ataka, A. Seki, Advantest Laboratories

1.2 Test-Yield Improvement of High-Density Probing Technology Using Optimized Metal Backer with Plastic Patch

1.3 RF MEMS Switches for Wide I/O Data Bus Applications
W. Tang, M. Cohn, K. Saechau, M. Whitlock, D. Brennan, MicroAssembly Technologies

SESSION 2
Finding the Gems in the Test Data Mine
P. Maxwell, Aptina Imaging (Chair)

2.1 A Pattern Mining Framework for Inter-Wafer Abnormality Analysis
N. Sumikawa, L. Wang, University of California, Santa Barbara; M. Abadir, Freescale Semiconductors

2.2 Adaptive Testing—Cost Reduction Through Test Pattern Sampling
M. Grady, P. Nigh, B. Pepper, J. Patch, M. Degregorio, IBM

2.3 Predicting System-level Test and In-Field Customer Failures Using Data Mining
H. Chen, R. Hsu, P. Yang, J. Shyr, MediaTek

SESSION 3
2.5D/3D-IC DFT
E.J. Marinissen, IMEC (Chair)

3.1 Test and Debug Strategy for TSMC CoWoS Stacking Process-based Heterogeneous 3D-IC: A Silicon Case Study

3.2 Fault Diagnosis of TSV-based Interconnects in 3D Stacked Designs
J. Tyszer, Poznan University of Technology; J. Rajski, Mentor Graphics

3.3 A Graph-Theoretic Approach for Minimizing the Number of Wrapper Cells for Pre-Bond Testing of 3D-Stacked ICs
M. Agrawal, K. Chakrabarty, Duke University

4:00 p.m. – 5:30 p.m.

SESSION 4
Scan Compression for Large Designs
S. Ravi, Texas Instruments India (Chair)

4.1 Two-level Compression Through Selective Reseeding
P. Wohl, J. Waisukauski, F. Neuveux, G. Maston, N. Achouri, Synopsis; J. Colburn, NVIDIA

4.2 SmartScan - Hierarchical Test Compression for Pin-limited Low-Power Designs
K. Chakravadhanula, V. Chickermame, D. Pearl, A. Garg, R. Khrana, S. Mukherjee, P. Naragaj, Cadence Design Systems

4.3 EDT Bandwidth Management—Practical Scenarios for Large SOC Designs
J. Tszyr, J. Janicki, Poznan University of Technology; W-T. Cheng, Y. Huang, M. Kassab, N. Mukherjee, J. Rażski, Mentor Graphics; Y. Dong, G. Giles, Advanced Micro Devices

SESSION 5
Data Gathering and Diagnostics
TBD (Chair)

5.1 PADRE: Physically-aware Diagnostic Resolution Enhancement
Y. Xie, O. Poku, X. Li, R. Blanton, Carnegie Mellon University

5.2 Test Data Analytics—Exploring Spatial and Test-Item Correlations in Production Test Data
C-K. Hsu, F. Lin, K-T. Cheng, University of California, Santa Barbara; W. Zhang, X. Li, Carnegie Mellon University; J. Carulli, K. Butler, Texas Instruments

5.3 Process Monitoring Through Wafer-level Spatial Variation Decomposition
K. Huang, Y. Makris, University of Texas, Dallas; N. Kapp, Yale University; J. Carulli, Texas Instruments

4:00 p.m. – 5:30 p.m.

SESSION 6
DFT and Security
V. Chandra, ARM (Chair)

6.1 Differential Scan-Path: A Novel Solution for Secure Design-for-Testability
S. Munich, Universitat Politècnica de Catalunya-BarcelonaTech; M. Wamser, O. Guillon, G. Sigl, Technische Universität München-TUM

6.2 Don't Forget to Lock Your SIB: Hiding Instruments Using P1687
J. Dvorak, Southern Methodist University; A. Crouch, J. Potter, ASSET InterTech; A. Zygmuntowicz, M. Thornton, Southern Methodist University

6.3 SCAN-PUF: A Low-Overhead Physically Unclonable Function from Scan-Chain Power-Up States
B. Niewenhuis, R. Blanton, M. Bhargava, K. Mai, Carnegie Mellon University
8:30 a.m. – 10:00 a.m.

SESSION 7
3-D TSV Testing
S. Pateras, Mentor Graphics (Chair)

7.1 Uncertainty-aware Robust Optimization of Test-Access Architectures for 3D Stacked ICs
S. Deutsch, K. Chakrabarty, Duke University; E.J. Marinissen, IMEC

7.2 Delay Testing and Characterization of Post-Bond Interposer Wires in 2.5-D ICs
S-Y. Huang, L-R. Huang, National Tsing Hua University, Taiwan; K-H. Tsai, W-T. Cheng, Mentor Graphics

7.3 A Test Probe for TSV Using Resonant Inductive Coupling
R. Rashidzadeh, F. Basith, University of Windsor

10:30 a.m. – 12:00 p.m.

SESSION 8
Managing Test for Complex SOCs
P. Varma, Apache Design (Chair)

8.1 Self-Repair of Uncore Components in Robust System-on-Chips: An OpenSPARC T2 Case Study
Y. Li, E. Cheng, S. Makar, S. Mitra, Stanford University

8.2 Optimizing Redundancy Design for Chip-Multiprocessors for Flexible Utility Functions
D. Cheng, S. Gupta, University of Southern California

8.3 Fault Mitigation Strategies for CUDA GPUs
P. Prietto, S. Di Carlo, G. Gambardella, L. Martella, D. Rolfo, P. Trotta, Politecnico di Torino

2:00 p.m. – 4:00 p.m.

SESSION 9
Protocols/Methodologies for Test Time Reduction
B. Parnas, LTX-Credence (Chair)

9.1 A Functional Test of 2-GHz/4-GHz RF Digital Communication Device Using Digital Tester
K. Ichiyama, M. Ishida, K. Naganami, T. Watanabe, Advantest

9.2 Theory, Model, and Applications of Non-Gaussian Probability Density Functions for Random Jitter/Noise with Non-White Power Spectral Densities
D. Chow, M. Shimanouchi, M. Li, Altera

9.3 The Implementation and Application of a Protocol-aware Architecture
T. Lyons, G. Conner, S. Sullivan, J. Aslanian, Teradyne

9.4 Test Time Reduction with SATOM: Simultaneous AC-DC Test with Orthogonal Multi-excitations
D. Chen, Z. Yu, Iowa State University; K. Maniar, M. Nowrozi, Texas Instruments

2:00 p.m. – 4:00 p.m.

SESSION 10
Advances in Test Generation
B. Becker, University of Freiburg (Chair)

10.1 A Circular Pipeline Processing-based Deterministic Parallel Test Pattern Generator
K-W. Yeh, J-L. Huang, National Taiwan University; H-J. Chao, L-T. Wang, SynTest Technologies

10.2 On the Generation of Compact Test Sets
A. Kumar, S. Reddy, C. Wang, University of Iowa; J. Rajski, Mentor Graphics

10.3 Application of Under-Approximation Techniques to Functional Test Generation Targeting Hard-to-Detect Stuck-At Faults
M. Prabhu, J. Abraham, University of Texas at Austin

10.4 A Distributed Multicore Hybrid ATPG System
X. Cai, P. Wohl, Synopsys

2:00 p.m. – 4:00 p.m.

SESSION 11
Board Test Methods
E. Larsson, Lund University (Chair)

11.1 FPGA-based Universal Embedded Digital Instrument
J. Ferry, Teradyne

11.2 AgentDiag: An Agent-assisted Diagnostic Framework for Board-level Functional Failures
Z. Sun, L. Jiang, Q. Xu, The Chinese University of Hong Kong; Z. Zhang, Z. Wang, X. Gu, Huawei Technologies

11.3 Demystifying PDL—What Is It and What Is Its Impact on Current and Future Standards?
J. Rearick, AMD

11.4 BA-BIST: Board Test from Inside the IC Out
Z. Conroy, Cisco Systems: A. Crouch, ASSET InterTech

Ph.D Thesis Competition Forum: Final Round
Y. Zorian, Synopsys (Chair)

PTF1 High-Sensitivity Test Signature for Unconventional Analog Circuit Test Paradigms
S. Sindia, V. Agrawal, Auburn University

PTF2 Nonintrusive Embedded Sensors for RF Circuit Test
L. Abdallah, H-G. Stratigopoulos, S. Mir,TIMA Laboratory

PTF3 Fault Modelling and Diagnosis for Nanometric Analog/Mixed-Signal/RF Circuits
K. Huang, University of Texas at Dallas
8:30 a.m. – 10:00 a.m.

SESSION 12
Novel Techniques for ADC and RF
M. Slamani, IBM (Chair)

12.1 Accurate Full-Spectrum Test Robust to Simultaneous Noncoherent Sampling and Amplitude Clipping
S. Sudani, L. Xu, D. Chen, Iowa State University

12.2 Zero-Overhead Self-Test and Calibration of RF Transceivers
A. Naxeray, J. Jeong, S. Otrv, Arizona State University

12.3 In-System Diagnosis of RF ICs for Tolerance Against On-Chip In-Band Interferers
N. Azuma, T. Makita, S. Ueyama, M. Nagata, Kobe University; S. Takahashi, M. Murakami, K. Hori, Renesas; S. Tanaka, M. Yamanouchi, Tohoku University

SESSION 13
Monitoring and Mitigating Aging
M. Tehranipoor, University of Connecticut (Chair)

13.1 A Design-for-Reliability Approach Based on Grading Library Cells for Aging Effects
S. Arama, M. Noorani, University of Texas at Dallas; J. Carulli, Jr., K. Butler, V. Reddy Texas Instruments

13.2 Representative Critical-Path Selection for Aging-induced Delay Monitoring
F. Firooz, M. Tahoori, Karlsruhe Institute of Technology; F. Ye, K. Chakrabarty, Duke University

13.3 Early-Life Failure Detection Using SAT-based ATPG

1:00 p.m. – 2:30 p.m.

SESSION 14
Reliability and Test of FPGAs and Memories
F. Frederick, ARM (Chair)

14.1 Module Diversification: Fault Tolerance and Aging Mitigation for Runtime Reconfigurable Architectures
H. Zhang, L. Bauer, J. Henkel, Karlsruhe Institute of Technology; M. Kochte, E. Schneider, C. Braun, M. Imhof, H-J. Wunderlich, University of Stuttgart

14.2 On the Reuse of Read- and Write-Assist Circuits to Improve Test Efficiency in Low-Power SRAMs
L. Zordan, A. Bosio, L. Dillido, P. Girard, A. Todri, A. Virazel, LIRM; N. Badereddine, Intel

14.3 Towards Data Reliable Crossbar-based Memristive Memories
A. Ghofrani, M. Lastra-Montes, K-T. Cheng, University of California, Santa Barbara

SESSION 15
DFT Advances
H. Konuk, Broadcom (Chair)

15.1 Diagnosis and Layout-aware (DLA) Scan-Chain Stitching

15.2 Design Rule Check on the Clock Gating Logic for Testability and Beyond
K-H. Tsai, S. Sheng, Mentor Graphics

15.3 ATE Test Time Reduction Using Asynchronous Clocking
P. Venkataramani, V. Agrawal, Auburn University
Advanced Industrial Practices (AIP) sessions provide an opportunity for attendees to learn the latest methods and techniques used by industry leaders in addressing some of today's most important test challenges.

**Wednesday 8:30 a.m.–10:00 a.m.**

**AIP SESSION 1**
Post-Silicon Validation and Debug  
E. Rentschler, AMD (Chair)

A 1.1 Validation Relevance, Challenges, Opportunities and Quick Wins  
M. Lowe, Samsung

A 1.2 Is Silicon Another (the Last) Verification Engine?  
S. Bailey, Mentor Graphics

A 1.3 Post-Silicon Validation and Debug Challenges: Scaling from SOCs to Servers  
C. Fleckenstein, Intel

**AIP SESSION 2**
On-Chip Monitoring and Sensing  
M. Tahoori, Karlsruhe Institute of Technology (Chair)

A 2.1 Critical Path Monitor Calibration and Characterization in a Multicore Processor  
A. Drake, IBM

A 2.2 On-Chip Sensing for Reliability  
M. Pont, Intel

A 2.3 Efficient In-situ Online Timing Slack Monitoring  
V. Chandra, ARM

**Wednesday 10:30 a.m.–12:00 p.m.**

**AIP SESSION 4**
Low-Cost Test with High-end Testers  
S. Davidson, Oracle (Chair)

A 4.1 Massive Multisite for Low-Cost Test  
S. Comen, Texas Instruments; M. Brophy, LTX

A 4.2 Lower-Cost Test Solution for CMOS Image Sensor Wafer Sort  
D. Rajakumar, S.K. Satish, Tessolve Semiconductor

A 4.3 Challenges with Development of High-end Testers for Lower Test Cost  
S. Desai, Texas Instruments; B. McCoy, Teradyne

**Thursday 9:00 a.m.–10:30 a.m.**

**AIP SESSION 5**
System-level Test Equipment  
B. Bartlett, Advantest (Chair)

A 5.1 Wireless Aspects of System Level Test  
C. Olgaard, LitePoint

A 5.2 SLT on ATE—Challenges and Vision  
D. Armstrong, Advantest

A 5.3 System-level Test Using Protocol-aware ATE  
S. Molavi, Broadcom

**Thursday 3:00 p.m.–4:30 p.m.**

**AIP SESSION 6**
Experiences with System-level Test  
X. Gu, Huawei Technologies (Chair)

A 6.1 System-level Testing for High-Volume Consumer Products  
H. Chen, C. Hsiao, W. Hsueh, R. Yang, MediaTek

A 6.2 Application of System-level Test to Multiple Industrial Designs  
S. Biswas, NVIDIA

A 6.3 System-level Test As Part of a Debug Strategy  
C. Fleckenstein, Intel
Tuesday 2:00 p.m.–3:30 p.m.

LECTURE 1
Elevator Talks
S. Mitra, Stanford University (Chair)

The always-popular set of short talks from academics on their latest research.

J. Abraham, University of Texas at Austin
N. Dutt, University of California, Irvine, USA
M. Fujita, University of Tokyo, K. Chakrabarty, Duke University
S. Gupta, University of Southern California
M. Hashimoto, Osaka University
S. Hellebrand, University of Paderborn
S. Komatsu, University of Tokyo
X. Li, Chinese Academy of Sciences
M. Maniatakos, New York University, Abu Dhabi
Z. Peng, Linkoping University
Y. Sato, Kyushu Institute of Technology
L-C. Wang, University of California, Santa Barbara
C-W. Wu, National Tsing-Hua University

Wednesday 8:30 a.m.–10:00 a.m.

LECTURE 2
Advanced Measurement Techniques
G. Maston, Synopsys

L 2.1 Practical Methods for Extending ATE to 40 and 50 Gbps
D. Keezer, A. Majid, T-H. Chen, Georgia Institute of Technology; C. Gray, L3Com Display Systems

L 2.2 An Enhanced Procedure for Calculating Dynamic Properties of High-Performance DAC on ATE
M. Lu, Advantest

L 2.3 A Novel Test Structure for Measuring Variance of Threshold Voltage in MOSFETs
T. Yamaguchi, Advantest Laboratories; J. Tandon, S. Komatsu, K. Asada, The University of Tokyo

Wednesday 2:00 p.m.–4:00 p.m.

LECTURE 3
Hardware Security and Trust
O. Sinanoglu, New York University Abu Dhabi (Chair)

L 3.1 Physical Analysis for Hardware Assurance
P. Song, IBM T. J. Watson Research Center

L 3.2 Security and Hardware-Software Interface
M. King, Intel

L 3.3 Security Evaluation of IC Camouflaging
J. Rajendran, O. Sinanoglu, R. Karri, New York University

L 3.4 Counterfeit Electronics: A Rising Threat in the Semiconductor Manufacturing Industry
K. Huang, Y. Makris, University of Texas at Dallas; J. Carulli, Texas Instruments

Lecture 3 Mini Panel
Research for Secure and Trustworthy Semiconductors
C. Merzbacher, SRC (Moderator)

Thursday 1:00 p.m.–2:30 p.m.

LECTURE 4
Test Methods for HF Signals
A. Chatterjee, Georgia Institute of Technology (Chair)

L 4.1 Performance Enhancement of a WCDMA/HSDPA+ Receiver via Minimizing Error Vector Magnitude
W. Gao, C. Liu, Broadcom

L 4.2 12-Gbps SerDes Jitter Tolerance BIST in Production Loopback Testing
Y. Cai, L. Fang, I. Chan, M. Olsen, K. Richter, LSI

L 4.3 Advanced Method to Refine Waveform Smear by Jitter in Waveform Sampler Measurement
H. Okawara, Advantest
PO 1 Simultaneous Secured Memory Built-in Self-Test in Heterogeneous Multicore Integrated Circuit
A. Srivastava, Freescale Semiconductor

PO 2 Design-for-Test, Diagnosis and Repair for Robust STTRAM Arrays
S. Ghosh, University of South Florida

PO 3 Phase Noise Measurement with Sigma-Delta TDC
H. Kobayashi, D. Hirabayashi, Y. Osawa, N. Harigai, T. Yamaguchi, N. Takai, Gunma University; O. Kobayashi, STARC; K. Niitsu, Nagoya University

PO 4 Assertions in Library ATPG Models for Robust Scan Patterns
S. Bahl, P. Gupta, H. Kaur, M. Jain, STMicroelectronics; K. Abdel-Hafez, S. Talluto, Synopsys

PO 5 Energy-centric Error Model of SRAM
S. Ghosh, University of South Florida

PO 6 Defect Analysis and Fault Modeling for Rnv8T Nonvolatile SRAM
B-C. Bai, C-A. Chen, Y-W. Chen, M-H. Wu, K-L. Luo, C-L. Hsu, L-C. Cheng, ITRI; C-M. Li, National Taiwan University

PO 7 Structural Universal Test Content
J. Bowling, Intel

PO 8 Layout-aware Weighted Bridge/Open Fault Coverage Considering Multiple Defect Sizes
M. Arau, Nihon University; K. Iwashiki, Tokyo Metropolitan Univ.

PO 9 Using Scan Diagnosis and Rule Weights to Characterize DFM Rule Performance

PO 10 Service-oriented Nonvolatile Memories
M. Indaco, S. Di Carlo, P. Prinetto, Politecnico di Torino

PO 11 Hierarchical Multi-Agent Approach for DFx Logic Verification in APUs
D. Akselrod, J-A Cruz-Pastora, F. Urrea, AMD

PO 12 Fast Scan-based On-Chip Delay Measurement Using Multiple Asynchronous Transfer Scan Chains
K. Katoh, Tsukuba National College of Technology

PO 13 Analysis and Test Methodology to Screen Memory-State-specific Parametric Leakage Failures in 28 nm
S. Dasturkar, P. Seeram, P. Bhadri, Qualcomm

PO 14 Test Pattern Modification for Average IR-drop Reduction
J. Li, W-S. Ding, H-Y. Hsieh, National Taiwan University; X. Wen, Kyushu Institute of Technology

PO 15 Analysis of Top-Off ATPG for Stuck, Transition, UDFM and SDD Faults
A. Gill, D. Walker, Texas A&M University; T. Olsen, AMD

PO 16 SRAM Vmin Analysis and Test Guard Band
J. Lee, C. Yeo, P. Chia, Cisco Systems

PO 17 IBM High-Throughput Parallel Parametric Tester Implementation and Smart Test Macro Design for Parallel Testing

PO 18 OCC Integration for Lower Test Cost and Higher Design Margin!
B. Rajanarayanan, SmartPlay Technologies

PO 19 Detection of Ground-Pin Open-Failure in a ZIF Connector Between Probe Card and ATE
G-Y. Kim, W. Nah, Sungkyunkwan University; S. Yoo, H-J. Kim, S. Park, Samsung

PO 20 The LYING Venn Diagram
S. Blanton, Carnegie Mellon University

PO 21 Method for Optimizing Test Time and Escape Rate for a Multivariate Failure Mode
J. Appleyard, N. Chadwick, M. Carlson, IBM

PO 22 Study of an Automated 77-GHz Automated Radar On-Wafer Test Solution
J. Nowakowski, STMicroelectronics

PO 23 An Efficient Approach for Intra-Cell Scan Chain Diagnosis
Z. Sun, A. Bost, L. Dilillo, P. Girard, A. Todri, A. Virazel, LIRMM, STMicroelectronics

PO 24 A Test-driven Methodology for Real-Time Online Temperature Prediction and Power Estimation
J. Kang, M. Cho, S. Yalamanchili, S. Mukhopadhyay, Georgia Institute of Technology

PO 25 Counterfeit Electronics: A Rising Threat in the Semiconductor Manufacturing Industry
K. Huang, Y. Makris, University of Texas, Dallas; J. Carulli, Texas Instruments

PO 26 Emerging Test Standards
IEEE Standards Working Group Representatives

Posters nominated by the Asian Subcommittee and associated with Panel 3.

PO 27 In-place Signal and Power Noise Waveform Capturing Within 3D Chip Stacking
M. Nagata, S. Takaya, Kobe University; H. Beda, *ASET

PO 28 Development of Testing Technology for Wide Bus Chip-to-Chip Interconnection in 3D LSI Chip Stacking System
M. Aoyagi, F. Imura, S. Melamed, S. Nemoto, N. Watanabe, K. Kikuchi, H. Nakagawa, National Institute of Advanced Industrial Science and Technology (AIST); M. Hagimoto, Y. Matsunuma, TOPS Systems

PO 29 Testability of Open Defects at Interconnects in 3D ICs with a Built-in Test Circuit for Supply Current Testing
S. Umezu, M. Hashizume, K. Takaya, W. Ikeda, National Taiwan University and Technology

PO 30 Time-to-Digital Converter Embedded in Boundary-Scan Circuit and Its Application to 3D IC Testing
H. Sakurai, H. Yotsuyanagi, M. Nakamura, M. Hashizume, University of Tokushima

PO 31 Test Access Mechanism for TSV Characterization in 3D ICs

PO 32 University Research in 2.5/3D IC Test and Design-for-Testability
K. Chakrabarty, M. Agrawal, S. Deutsch, B. Noia, R. Wang, Duke University

PO 33 Design Guidelines for System-level Test

PO 34 How to Deal with RAM Errors at System Level?
K. Li, Huawei Technologies

PO 35 Using a Component-based DRAM Area, Power, and Timing Modeling Tool (DARt) for Fast Variation Analysis
H-C. Shih, C-W. Wu, National Tsing Hua University; P-W. Luo, J-C. Yeh, S-Y. Lin, D-M. Kwai, Industrial Technology Research Institute; S-L. Lu, A. Schaefer, Intel
The Corporate Forum track will be on Tuesday and Wednesday in a comfortable meeting area adjacent to the exhibits floor. This will integrate the presentations more cohesively with traffic from the ITC exhibition. As in previous years, our Diamond Supporter plans to provide a 1-hour presentation on Tuesday morning followed by a hosted lunch. The remaining presentations will start at 1 p.m. at 20-minute intervals on Tuesday. Further presentations will be on Wednesday. The schedule will minimize conflict with the conference technical program. The 20-minute length allows attendees to enjoy multiple presentations in a short time span and runs at a fast pace to keep this event more interesting. Scheduling is setup to maximize attendance.

This marketing tool is provided free of charge for exhibitors and supporters to present the latest developments from their companies, and promote their activities at ITC.

**Tuesday 11:00 a.m.–12:00 p.m.**

11:00 a.m. **OptimalTest**  
NVIDIA presentation: Leveraging Cross-Operational Test Data for Manufacturing Yield and DPPM/RMA Improvements

**Tuesday 1:00 p.m.–2:00 p.m.**

1:00 p.m. **GOEPEL Electronics**  
Embedded System Access for Test at Chip, Board and System Level

1:20 p.m. **Advantest**  
CloudTesting™ Service: Revolutionary new Concept for Post-Silicon Validation

1:40 p.m. **DCG Systems**  
ELITE: Lock-in Thermography Overview

**Wednesday 12:20 p.m.–1:40 p.m.**

12:20 p.m. **ASSET InterTech**  
ScanWorks—Embedded Instrument Test and Debug Platform

12:40 p.m. **Chroma ATE**  
Advanced Tri-Temp, No LN2 Attached—Can Your SMU Do This?

1:00 p.m. **Roos Instruments, Inc.**  
True HVM Testing Beyond 20 GHz

1:20 p.m. **Evans Analytical Group**  
ATE Test Services
Monday, 4:30 p.m. – 6:00 p.m.

PANEL 1 The Future of Test Automation —Where Should We Place Our Bets?
W. Eklow, Cisco (Moderator) • C. Pyron, Freescale Semiconductor (Organizer)

This executive panel will look at the key challenges facing specialized test automation vendors as they engage with today's semiconductor market. Participants will share their views on market forces, impact of standards, and the future of the industry.

Panelists: C.J. Clark, Intellitech • H. Ehrenberg, Goepel • P. van den Eijnden, JTAG Technologies • J. Johnson, SiliconAid • G. Woppman, ASSET InterTech

Reception/Social follows.

Tuesday, 4:00 p.m. – 5:30 p.m.

PANEL 2 Where Are the Waldos of DFT
J. Abraham, University of Texas (Moderator) • R. Aitken, ARM (Organizer)

Whatever happened to the promised revolutions in DFT? Full-chip logic BIST, 1000X compression, defect-based testing, partial scan, and more. Our panel discusses why they are hard to find now and where they might be in the future.

Panelists: S. Davidson, Oracle • P. Maxwell, Aptina • S. Ozev, Arizona State University • J. Rajski, Mentor Graphics • J. Rearick, AMD

Wednesday, 10:30 a.m. – 12:00 p.m.

PANEL 3 Where Is 3-D Test Going? Is It a New Mainstream or a Marginal Trend?
W. Eklow, Cisco Systems (Moderator) • Y. Sato, Kyushu Institute of Technology (Organizer)

3-D is a very hot topic and various technologies are proposed. Where is it going? Is it a new mainstream or a marginal trend? This panel debates about what should be best strategies and what problems are still open. A poster session linked with this panel also shows current movements.

Panelists: K. Chakrabarty, Duke University • K.-Y. Chung, Samsung • S. Goel, TSMC • M. Koyanagi, Tohoku University • E.J. Marinissen, IMEC

Thursday, 3:00 p.m. – 4:30 p.m.

PANEL 4 Challenges of SerDes and DDR Defect Testing and AC Spec Measurements
G. Fleeman, Advantest (Moderator) • E. Atwood, IBM (Organizer)

With the rapidly evolving capability of link architectures, how has manufacturing test been adapting and what is being done to ensure ongoing quality? Is there a best method for functionally testing Serial and DDR links? External loopback is used in the board level environment and at module test. What are the issues in performing these tests and are there alternatives? Which AC specification measurements are acquired and how are they acquired?

Panelists: A. Burgmeier, Freescale Semiconductor • M. Li, Altera • G. Roberts, McGill University • R. Salazar, Intel • M. Tirupattur, Analogbits

PANEL 5 The Battle of the Standards
S. Adham, TSMC (Moderator) • R. Kapur, Synopsys (Organizer)

Three IEEE standards are developed to address test problems at different integration levels (core, chip and system). These standards overlap in some aspects and might complement each other in others. In this panel, IEEE test standards experts will debate the value of each standard and present the infrastructure required to use the standard in a design. Panelists will also provide their view if and how all these standards may co-exist in the future.

Panelists: C.J. Clark, Intellitech • A. Cron, Synopsys • T. McLaurin, ARM • J. Rearick, AMD
IEEE Computer Society Test Technology Technical Council Workshops

Thursday and Friday

General Workshop Information
Three workshops are being held in conjunction with ITC 2013. The embedded DATA workshop is a one-day workshop that runs from 8:00 a.m. to 4:30 p.m., in parallel with the ITC sessions, on Thursday, September 8; whereas the two others, 3D-TEST and TVHSAC, run immediately after the last session of ITC. These latter two two-day workshops hold a reception for their participants on Thursday evening, and continue their technical sessions on Friday, September 13. The technical scope of each workshop is described below.

Workshop Registration
All workshop participants require registration. To register in advance for one of the workshops, do so online or by faxing the download form. Otherwise, register onsite at regular rates at the ITC registration counter at the Disneyland Hotel Conference Center during Test Week. Admission for onsite registrants is subject to availability. Discount workshop registration rates apply until August 16, 2013. See page 25 for details. Workshop registration includes the technical sessions, digest of papers, break refreshments and corresponding meals. The DATA workshop meal will be lunch at noon in the ITC exhibit hall. Participants in the 3D-TEST and TVHSAC workshops will have a reception on Thursday evening and lunch at noon on Friday.

Digest of Papers
A digest of papers will be distributed only to attendees at the workshops as an informal proceedings.

Two-Day Workshop Schedule
Both two-day workshops will adhere to the same schedule:

**Thursday, September 12**
- Registration: 2:00 p.m. – 5:00 p.m.
- Opening Address: 4:30 p.m. – 5:00 p.m.
- Technical Session: 5:00 p.m. – 7:00 p.m.
- Reception: 7:30 p.m. – 9:30 p.m.

**Friday, September 13**
- Technical Sessions: 8:00 a.m. – 4:00 p.m.

*Note: Workshop schedule is subject to change*

Further Information
For more information on the three workshops contact their organizers by e-mail or check the TTTC Web site [http://computer.org/tttc](http://computer.org/tttc)

WORKSHOP RECEPTION
Thursday, September 12
7:30 – 9:30 p.m.
DATA: IEEE International Workshop on Digital and Analog Test and Data Analysis

This workshop is embedded in the ITC program and has different registration rates than the two-day workshops. It runs from 8:00 a.m. to 4:30 p.m. on Thursday.

Scope: Every testing of digital logic has made significant improvements in recent years with the use of the stuck-at and delay fault models. Advances in digital test have now led the way to analog and mixed-signal test, looking at analog fault modeling and coverage, testing and protocols, and also issues like power droop and crosstalk in digital logic. New data mining techniques such as outlier analysis and adaptive test have helped to improve quality by exploiting IC defects that have “analog” signatures, even in digital devices. However, our capability for data analysis, defect modeling, simulation and fault coverage of analog logic has not kept up with capabilities in the digital domain. Besides presentations on “classical” digital product engineering, this year’s workshop is intended to focus on new techniques for data analysis of analog circuits, or for the analog behavior of digital logic. Suggested topics include:

- Outlier identification
- Analog effects in digital logic
- Advanced product engineering techniques
- Data-driven testing
- Yield-learning and analysis
- Embedded instrumentation testing
- Data analysis methods
- Advanced dppm reduction techniques
- Product and project case studies
- Adaptive test for product engineering
- Analysis of aging and reliability
- Fault localization and diagnosis

General Chair: Arani Sinha, Arani.Sinha@intel.com
Program Chair: Jeff Roehr, JLRoehrTI.com

3D-TEST: 4th IEEE International Workshop on Testing Three-Dimensional Stacked ICs

Scope: The fourth 3D-TEST Workshop focuses exclusively on test of and design-for-test for three-dimensional stacked ICs (3D-SICs), including systems-in-package (SIP), package-on-package (POP), 3D-SICs based on through-silicon vias (TSVs), microbumps and/or interposers. While 3D-SICs offer many attractive advantages with respect to heterogeneous integration, smaller form-factor, higher bandwidth and performance, and lower power dissipation, there are many open issues with respect to testing such products. The 3D-TEST Workshop offers a forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike. Topics to include:

- Defect due to wafer thinning
- Known-good die /stack testing
- Test flow optimization for 3D-SICs
- Defect in intra-stack interconnects
- Reliability for 3D-SICs
- Tester architecture for 3-D testing
- DFT architecture for 3D-SICs
- Standardization for 3-D testing
- TSV test, redundancy, and repair
- Failure analysis for 3D-SICs
- Test cost modeling for 3D-SICs

General Chair: Yervant Zorian, zorian@synopsys.com
Program Chair: Erik Jan Marinissen, erik.jan.marinissen@imec.be

TVHSAC: 3rd IEEE International Workshop Test and Validation of High-Speed Analog Circuits

Scope: Demand for higher bandwidths never lets up in the world of communication and networks. While we struggle today to make 40-Gbps line-rates a reality, plans are already afoot for 400 Gbps. Similarly, in wireless communications, 60 Ghz is coming online today, but designers are already planning the next few generations up to THz. What is high speed? It clearly depends: on the medium of transmission, on power constraints, on process technology, on link parallelism, on cost and quality requirements and on the electrical and thermal environment of operation. These constraints define a multidimensional box that designers are placed in and asked to provide the highest bandwidth they can, inside a room whose walls seem constantly to move inwards. A lot of the functionality is increasingly analog with strict standards regulating their design and use. And it is a race with no end in sight. The IEEE Workshop on Test and Validation of High-Speed Analog Circuits is designed to address a big aspect of this race: cost and quality. Increasing speed has given rise to a spike in complexity of analog circuits. This has been further stressed by the need for integrating with digital functionality in SOCs. Whether embedding in monolithic dice or integrating in a SIP, integration has thrown its share of problems. Defect coverage alone is no longer sufficient to qualify a die. We need parametric coverage, as early in the manufacturing flow as possible. This workshop addresses defect and parametric coverage of all analog circuits involved in making high bandwidth communications a reality. The scope of the workshop includes, but not limited to:

- Analog DFT and test methods
- High-speed PLL test and characterization
- ATE for high-speed analog measurement
- SERDES test and characterization
- Self-healing and self-calibration techniques
- On-die high-speed sensors and test structures

General Chair: Amit Majumdar, Amit.Majumdar@xilinx.com
Program Chair: Haralampos Stratigopoulos, haralampos.stratigopoulos@imag.fr
Monday 6:00 p.m. – 7:30 p.m.

**Monday Reception/Social**
*(Following Panel 1)*

Monday, September, 6:00 p.m. – 7:30 p.m.
Mark Twain Room in the Frontier Tower

Light food and beverages will be provided.
Sponsored by the IEEE Philadelphia Section.

Tuesday 6:30 p.m. – 8:00 p.m.

**ITC Grand Reception**

Tuesday, September 10, 6:30 p.m. – 8:30 p.m.
Magic Kingdom Lawn, Disneyland Hotel

Join us at our *California Summer*-themed event being held at a beautiful outdoor venue. Guests can socialize with friends old and new while enjoying food and drinks.
All Test Week activities require a registration badge for admittance. Register in advance online. Otherwise, register on-site at regular rates during Test Week at the ITC registration counter at the Disneyland Hotel Conference Center. See page 26 for registration hours. To obtain a substantial discount register no later than August 16, 2013.

**ITC Full-Conference Registration** Includes ITC technical paper and panel sessions, lecture and advance industrial application series, exhibits, ITC receptions, lunch in the exhibit hall, break refreshments, download ITC 2013 Proceedings and presentation slides, ITC tote and shirt. Registration does not include the tutorials on Sunday and Monday or the workshops on Thursday and Friday. May purchase additional download ITC 2013 Proceedings at $25 each; past proceedings CD-ROM set at $100.

**ITC One-Day Registration (Onsite-only)** Includes ITC technical program activities, exhibits, lunch in the exhibit hall and break refreshments—all for the day of registration only. Also includes ITC 2013 Proceedings and presentation slides, ITC tote and shirt. Registration does not include ITC welcome receptions. May purchase: additional download ITC 2013 Proceedings at $25 each; CD-ROM set at $100.

**ITC Free Exhibits-only Registration (Onsite-only)** Includes admission to exhibits on Tuesday, Wednesday and Thursday and corporate presentations on Tuesday. Lunch and receptions not included.

**Tutorial Registration** Includes one tutorial, study material and coffee breaks. Lunch will be provided for those attending consecutive tutorials on the same day, e.g., Tutorial 1 and Tutorial 4. The study material includes a hardcopy of the presentation material; and, when applicable, a relevant textbook (textbooks are provided to attendees who register at IEEE/CS member or nonmember rates). You may register for four events (two on Sunday and two on Monday). Registration does not include the ITC technical program, ITC receptions, exhibits, exhibit hall lunches, ITC publications, ITC tote, shirt or the workshops on Thursday and Friday.

**Workshop Registration** Includes the items specified on page 22. Registration does not include the ITC technical program, exhibits, ITC receptions, exhibits, exhibit hall lunches (except for the embedded workshop), publications, ITC tote, shirt or the tutorials on Sunday and Monday.

**Discount Rates** Early registration rates apply only when your completed registration form and payment are postmarked or faxed by August 16, 2013. Online registrations must also be received by this date. To receive IEEE/Computer Society member or student member reduced rates, you must include your member number, which will be verified.

**Student Rates** IEEE student members must also present their current IEEE Student Member card at the ITC registration counter. Student nonmembers must present their current school student ID.

### Registration Fees

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*not available after August 16, 2013, †Online registration not available.

### Refunds

Registration fees paid by August 16, 2013 are refundable on written request to ITC, c/o BADGEGuys, 1959 Jester Circle, Lawrenceville, GA 30043 USA, postmarked or faxed (+1 678.669.1802) by August 16, 2013. A $75 processing fee is charged for each refund.
Registration for All Activities

ITC registration counter at the Disneyland Hotel Conference Center

Sunday, September 8 to Thursday, September 12
7:30 a.m. – 5:00 p.m.

Need More Registration Information?
Contact the ITC office
2025 M Street, NW, Suite 800, Washington, DC 20036, USA
Tel. +1 202.973.8665    Fax. +1 202.973.8716

Fringe Technical Meetings
ITC arranges for meeting space for appropriate IEEE- or Computer Society TTTC-sponsored groups wishing to hold their meetings during Test Week, September 8 – 12. Contact the ITC office.
ITC 2013 Proceedings Distribution

ITC proceedings will be delivered electronically.

All ITC full-conference and one-day attendees, including students, will receive access to the 2013 ITC online proceedings free of charge.

Preregistered Full-Conference Attendees
All preregistered full-conference attendees will receive an email containing a download link a few days before the conference when the proceedings become available.

Onsite Full-Conference and One-Day Attendees
Full-conference and one-day attendees registering onsite will receive the download link at the time of registration.

Ordering Additional Proceedings with Advance Registration
All preregistered full-conference attendees may also order additional download 2013 proceedings, beyond the free copy, at $25 each.

Purchasing Additional Proceedings at the Conference
Full-conference and one-day attendees may also purchase onsite additional downloads of the 2013 proceedings for $25 each.

New This Year

ITC 2013 Technical Paper Presentations
Available free for download along with proceedings

The ITC Program Committee has compiled the slides used for this year’s technical paper presentations—including lectures and advanced industrial practices*—and has them available for download. You can review sessions that you attended and cover those that you could not attend. The summaries of the poster presentations will also be included. This will only be available as a download to registered full- and one-day conference attendees, including students—one per person. Preregistered attendees will receive a download link a few days before the conference. Others will receive the link when they register onsite.

The paper presentation slides make the perfect complement to the full manuscripts in the proceedings, as they contain the latest data.

*Some authors have chosen not to participate. These omitted papers will be identified. Slides used in panel sessions and the corporate forum are not included.

ITC Proceedings Five-Year Set
Five ITC CD-ROM proceedings for the years 2011, 2010, 2009, 2008 and 2007 are being sold as a set for $100. The set can be ordered with your online registration for pick-up at the conference or purchased onsite. One set per attendee. Quantities are limited.
Reserve a Disneyland Hotel room online by clicking the button above.

1. Rooms may be reserved for the period from **September 5, 2013 to September 16, 2013**

2. Cancellation: Disneyland Hotel's policy is that guests must cancel or change their reservation more than 72 hours prior to arrival (three full days prior to the scheduled date of arrival). Cancellations will be subjected to a penalty fee equal to one night's room rate and tax if less than 72 hours notice is given.

3. The reservation cutoff date is **August 16, 2013 at 5:00 p.m. EDT**. Reservations made after that date will be made at the ITC rate on a space-available basis.

4. **Discounted Disneyland theme park tickets** may be purchased when you make your reservation. The online store for tickets is open from **July 3, 2013 until 9:00 p.m. PST on Thursday, September 5, 2013**. Tickets are valid from **September 3, 2013 to September 16, 2013**.

5. Parking for hotel guests is $15/night for self-parking and $22/night for valet parking. Follow the "Hotels" signs directly to your destination; do not park in a theme park lot. Those staying at the Disneyland Hotel should park in the **Fantasy parking lot**.

6. Sleeping rooms provide free Internet access.

7. If you need assistance or have questions with hotel reservations, please contact Connections Housing at 404.918.9129. The main contact at Connections is **Jay Pierce** (jay@connectionshousing.com).

**Click here** for more hotel information, location and driving instructions.

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**Disneyland Hotel Rate**
(exclusive of taxes and fees)

**Standard Room $174.00**
(for up to four people)

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**Message to Attendees:** ITC has made every effort to secure the best possible group nightly room rate for you at this event. That rate results from a negotiated overall package of event needs such as sleeping rooms, meeting room space and other requirements. Contracts with the venue include a provision to reduce event costs if ITC meets or exceeds its minimum sleeping room block guarantee. Conversely, event costs will increase if ITC falls short of its minimum room block guarantee. Please help ITC keep the costs of this event as low as possible by booking your housing needs at the designated host hotel and through the reservation process created by ITC. Reserving elsewhere means you are booking outside the contracted room block, jeopardizing ITC's ability to meet its contracted obligations and to keep registration fees to a minimum. ITC appreciates your support and understanding of this important issue. Thank you.
Location

The ITC conference and all associated Test Week events will be held at the Disneyland Hotel Conference Center in the Disneyland Resort, Anaheim, California. The Disneyland Hotel, our conference hotel, is only a short walk to the Disneyland and California Adventure theme parks with their popular rides and attractions. (Discount theme park tickets are available online from July 3, 2013 until September 5, 2013.) You can also walk to the nearby Downtown Disney area, a lively promenade featuring unique shopping and dining, as well as nighttime entertainment.

Travel

Air

The three airports in closest proximity to the Disneyland Resort are Orange County (John Wayne) Airport (SNA), Long Beach Airport (LGB) and Los Angeles International Airport (LAX). There are several transportation options from these airports to the Disneyland resort. ITC has set up the discount fares for travel to/from airports.

Disneyland Express Bus

The Disneyland Express is a full-size motor coach that operates between the resort and John Wayne (SNA) and Los Angeles International (LAX) airports. A discount fare coupon is available for ITC participants.

SuperShuttle

SuperShuttle shared-ride van service available at all airports. An ITC discount fare is offered for reservations that are made and paid online. You may also arrange for your trip without a reservation (at regular rates) upon arrival at the airport. Reservations for travel to the airport should be made the day before your departure.

Limousine

Limousine service by Best Chauffeured Worldwide is available from all of Southern California for any transportation needs. Click here to make a reservation.

Taxi

Taxi service is available at all airports. Some offer flat-rate fares to the Disneyland resort.

Car

See the Disneyland Web site for driving instructions. Registered hotel guests at a Disney Resort hotel should follow signs to their hotel’s parking lot. Those staying at the Disneyland Hotel park in Fantasy parking lot. Attendees not staying at a Disney hotel should also park in the Fantasy parking lot. A daily self-parking fee of $15 is charged. Valet parking is available at hotel entrances for $22 per day.
The ITC Advance Program release 8.0 was generated with Adobe Acrobat 8.2.6 on 6-September-2013.

The program will be updated periodically as new material is available—check back often.

Navigate using the tabs at the top of each page.

Use underlined links in the At-a-Glance to find specific items.

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