General Instructions for ITC 2024 Posters

This file contains instructions to prepare and upload your poster-related files. Please read all instructions carefully.

1. **Poster session time and place:** The poster session will be held from **12:00 p.m.–02:00 p.m.**, **November 06 (Wednesday) 2024** (tentative; kindly check the official ITC website regularly for the exact date and time), on the exhibition floor of ITC 2024. Note that the posters should be hung anytime Wednesday, AM.

2. **Submission link:** The link to upload your files is given below, where you will also be requested to fill in your information and a release consent form.

   https://forms.gle/H5HG81K4FtTMnVvA6

   The deadline (firm) for filling out the form and uploading your poster file is **October 2nd, 2024.** Because we will have a physical poster session, each poster presenter needs to present in person during the session.

   (**Required**) 1-page **3'x4'** (90.7 cm by 121 cm) **portrait poster (4' in height)** (PDF).

   Samples or guidelines for posters can be found at http://www.itctestweek.org/itc-authors-page/. **File name:** start the file name with your poster ID, such as "PO.X poster". Replace X with your poster ID. Your poster ID can be found in the table attached at the end of this file.

3. **Printing poster:**
   - (Default) Print it by yourself and bring it to the conference site,
   - (Option) ITC uses **Pinnacle Exposition Services LLC** (web: https://pinnacle-expo.com / email: posters@pinnacle-expo.com / phone: **1-855-451-6893**) to print banners. If you want to use them to print poster, please contact Pinnacle Exposition Services LLC directly. ITC does **NOT** provide the printing service. If you use their service, your poster will be shipped with other ITC banners to the conference site.
   - (Option) You can also find a local print service (e.g. Fedex office at San Diego downtown – please google) and use them. Note: If you use Fedex service, you would select "mounted poster" with the size 36"X48'' "extra-large portrait". If you use a local service like this, you can pick it up yourself and bring it to the exhibit floor to set up the poster. ITC does **NOT** provide any pick-up service.

4. **Registration**:
   - All poster presenters must register ITC under the "**ITC Technical Conference Program Participant**" category. All presenters are expected to be physically present during the poster session on the exhibit floor.
   - The advance registration deadline is **October 2nd, 2024**.
   - A limited number of rooms in the hotel are available exclusively for ITC 2024 participants. The hotel booking deadline is also **October 2nd, 2024**. After the deadline, the hotel will NOT honor the ITC hotel rate any more.

List of Posters in ITC 2024

Poster ID	Submission #	Title
PO.1	16	Memory BIST for Automotive Non-destructive Memory Testing (short paper)
PO.2	19	Shift-left approach for SSN Oriented design: Enabling Robust RTL-Based SOC Automated Validation flow for ATPG and Power-Up Sequence
PO.3	42	Method for Diagnosing Clock Jitter Using FPGA
PO.4	51	(Short Paper) Efficient Noise Injection Methodology for Sample and Hold Circuits in AMS Behavioral Models
PO.5	62	Minimizing Probe Touchdown Route After First EDS Steps for Test Cost Reduction
PO.6	81	Improved Silent Data Error Detection through Test Optimization using Reinforcement Learning
PO.7	93	High-Performance ATPG with Loadable Nonscan Cells
PO.8	121	Test Time Optimization: A Novel Staggered-capture Architecture Using A Token-passing Architecture
PO.9	156	JTAG Protocol Aware Debug Tool for efficient debugging on V93K
PO.10	157	Inline Full Test Flow Scoping Capability on V93K Smart Scale
PO.11	158	Automation of PMU module using POP for TTR
PO.12	161	Evolution of PXI(e) Test for Digital Solutions
PO.13	162	UID Way Of End-To-End Specification Compliance And Data Analysis
PO.14	163	Internally generated scan resets using OCC
PO.15	164	Industrial application of IEEE P1687.2 for post-Si verification of a smart power device
PO.16	165	Efficiency and Reliability Enhancement in Pre-Silicon Validation Lessons from ASIC Networking product
PO.17	166	Bridging the EDA to ATE gap for mixed-signal with IEEE P1687.2 and P1450.1-2024
PO.18	167	Synergetic Pre- and Post-Silicon SLM Analytics for Reliable and Safe Automotive
PO.19	168	Optimizing Mobile & Automotive GPUs with Streaming Fabric, SEQ/XLBIST, IEEE1687 and TSO.ai
PO.20	170	Intel HDMT ATE Capabilities Poster
PO.21	171	Solving Verification Challenges for Modern DRAM based Systems requiring Refresh and Refresh Management Compliance
PO.22	172	Executable Tables, ‘Key’ Concepts Demonstrated Using DDR5 Speed Bin Example
PO.23	173	Enhancing test quality for abutted designs with Logic BIST
PO.24	174	Flexible Scan test Architecture with Scalable Bus in 2.5D/3D Packaged Chips
PO.25	175	Optimizing ATE Resources for WLAN Rx PER Testing: A Cost-Effective Approach
PO.26	176	A Novel Solution for Efficient Signal Pattern Debug of Complex Devices Interconnect

PO.27	177	Accelerated 3D IC DFT Development using commercial multi-die solution
PO.28	178	Improving WLAN Rx PER Test Efficiency for Increased ATE Yield
PO.29	179	Solving Memory Subsystem Verification Challenges for Multi-Instance Designs.
PO.30	180	Experimental Evaluation of Multi-Stage Jitter-Reduction Circuits for 54 GHz ATE Clocks
PO.31	181	Automation to Speed up the process of Timing Closure of the IJTAG Network
PO.32	182	Cell-aware Chain Diagnosis for Backside Power
PO.33	183	Layout-aware Chain Diagnosis for Backside Power
PO.34	184	AI Chip Testing: Transforming Challenges into Opportunities with AI/ML/LLM Technology
PO.35	185	Driving deterministic In-System Test using Advanced Peripheral Bus (APB)
PO.36	186	Enhanced Security Mechanism for 1687 Network
PO.37	187	1687 Solution for Tiled Based Design with Feedthroughs
PO.38	188	TDR-Based S-Parameter Estimation of Signal Transmission Line on ATE Utilizing Built-In Driver and Comparator
PO.39	189	Improved area overhead with advanced memory dump and memory test automation for AI chips
PO.40	191	Efficient Test port access to address test time
PO.41	192	Effective detection of uncommon faults by SMarchCHKBvcd algorithm
PO.42	193	Embedded Trace: A Key Enabler for Silicon Debug and Continuous Monitoring
PO.43	194	Scalable Multi-Chiplet Test Solution Using IEEE 1838
PO.44	195	Test Chip Design for Small Delay Defect Diagnosis Based on C-testable Arrays and Mutually Orthogonal Latin Squares