2025 INTERNATIONAL TEST CONFERENCE

September 21 - 26, 2025

SAN DIEGO, CA, USA

Call for Papers

The International Test Conference (ITC) is the world's premier venue dedicated to the electronic test of devices, boards and systems—covering the complete cycle from design verification, design- for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, reliability and failure analysis, and back to process and design improvement.

Authors are invited to submit original, unpublished papers describing recent work in the field of testing and testable design. Of particular interest are works dedicated to the topics listed on the right and/or works focused on special tracks such as **Automotive Reliability, Reliability of AI HW and usage of AI for Testing, 3D/2.5D and Chiplet Testing, or HW Security**. Authors are also invited to submit practical, industry-oriented papers.

A **special industrial case-study track** is dedicated to papers that enable others to learn best industrial practices.

Submissions must include:

- Title of paper.
- Name, affiliation, e-mail address of each author. (Double blind review is not required).
- The corresponding author(s). ITC will communicate with the corresponding author(s).
- One topic from the topic list.
- An electronic copy of a complete paper of 6~10 pages for regular papers (including regular Industrial case-study papers) or 3~5 pages for short Industrial Practices papers.
- An abstract of maximum 100 words to be entered online.

ITC maintains a competitive selection process for technical papers. Submissions must clearly describe the status of the reported work, its contribution, novelty and/or significance. Supporting data, results (priority is often given to papers with results from real designs) and conclusions, and references to prior work must also be included.

Paper title/abstract due:	**March 7, 2025**
Paper PDF due:	**April 2, 2025 (Extended)**
Author notification:	**May 13, 2025**
Final manuscript due:	**May 31, 2025**

Test Week tutorial and workshop proposals are also welcomed. Deadlines and other information about proposals can be obtained from TTTC at: http://tab.computer.org/tttc

For detailed information about the submission process, requirements and deadlines, the selection process, and any other questions regarding the program itself or contact information, please consult the ITC web site at http://www.itctestweek.org.

For further information:

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ITC invites submissions on the latest advances in test, validation, diagnosis and security of IPs, ICs, boards and systems.

Topics of interest include, but not limited to:

- 3D/2.5D Test
- 5G/6G Test
- Adaptive Test in Practice
- AI/Machine Learning in Test
- ATE/Probe Card Design
- Automotive Reliability
- Advances in Boundary Scan
- Built-In Self-Test
- Data Driven Test Methods
- Defect-oriented Testing
- Design for Test (DFT)
- DFM and Test Diagnosis
- Diagnosis
- Economics of Test
- End-to-End Data Analysis
- End-to-End System Security
- Emerging Defect Mechanisms
- Field Monitoring, Test, & Debug
- Hardware Security and Trust
- IoT Testing
- Jitter, High-Speed I/O and RF
- Test Known-Good-Die Test
- Memory Test and Repair
- MEMS Testing
- Mixed-Signal and Analog Test
- New Technologies and Test
- Online Test
- Pre-Silicon/Post-Silicon
- Verification Power Issues in Test
- Protocol-aware Test
- Quantum Device Testing
- Reliability and Resilience
- SoC/SiP/NoC Test
- Silent Data Corruption
- Silicon Debug
- Simulation and Emulation
- System Test (Applications)
- System Test (Hardware/Software)
- Test Compression
- Test-to-Design Feedback
- Test Escape Analysis
- Test Flow Optimizations
- Test Generation and Validation
- Test Resource Partitioning
- Test Standards
- Testing High Speed Optics/Photonics
- Timing Test
- Yield Analysis and Optimization

Program committee members:

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