

The International Test Conference (ITC) is the world's premier venue dedicated to the electronic test of devices, boards and systems—covering the complete cycle from design verification, design- for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, reliability and failure analysis, and back to process and design improvement.

Students are invited to submit original, unpublished papers describing recent work in the field of testing and testable design. Of particular interest are works dedicated to the topics listed on the right and/or works focused on special tracks such as **Automotive Reliability, Reliability of AI HW and usage of AI for Testing, 3D/2.5D and Chiplet Testing, or HW Security**. The student track is a new initiative of ITC25: a set of sessions will be dedicated to students' works, including oral presentations, roundtables with industrials and professors, career fair opportunities and the final of the McCluskey Doctoral Thesis Award contest.

Submissions must include:

- Title of paper.
- Name, affiliation, e-mail address of the student. (Double blind review is not required).
- An electronic copy of a complete paper of **2 pages**.
- References can exceed in and not out of page 3.
- An abstract of 110 words or less to be entered online.

Every student can submit one or more 2-page papers, which can be authored exclusively by the student. The two pages must provide the compact description of a complete methodology/strategy/design/concept, with minimal indispensable background and synthetic experimental results. The format must follow the templates approved by IEEE.

Poster submission deadline: Author notification:

May 20, 2025 June 15, 2025

The submission will be peer reviewed and the accepted 2-page papers will be indexed in **IEEE Xplore**.

Test Week tutorial and workshop proposals are also welcomed. Deadlines and other information about proposals can be obtained from TTTC at: <u>http://tab.computer.org/tttc</u>

For detailed information about the submission process, requirements and deadlines, the selection process, and any other questions regarding the program itself or contact information, please consult the ITC web site at <u>http://www.itctestweek.org.</u>

For further information:

General Chair

Jennifer Dworak

Southern Methodist University, US

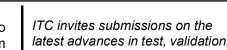
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ITC invites submissions on the latest advances in test, validation, diagnosis and security of IPs, ICs, boards and systems.

Topics of interest include, but not limited to:

3D/2.5D Test 5G/6G Test Adaptive Test in Practice AI/Machine Learning in Test ATE/Probe Card Design Automotive Reliability Advances in Boundary Scan **Built-In Self-Test** Data Driven Test Methods **Defect-oriented Testing** Design for Test (DFT) DFM and Test Diagnosis Economics of Test End-to-End Data Analysis End-to-End System Security Emerging Defect Mechanisms Field Monitoring, Test, & Debug Hardware Security and Trust IoT Testing Jitter, High-Speed I/O and RF Test Known-Good-Die Test Memory Test and Repair MEMS Testing Mixed-Signal and Analog Test New Technologies and Test Online Test Pre-Silicon/Post-Silicon Verification Power Issues in Test Protocol-aware Test Quantum Device Testing Reliability and Resilience SoC/SiP/NoC Test Silent Data Corruption Silicon Debug Simulation and Emulation System Test (Applications) System Test (Hardware/Software) Test Compression Test-to-Design Feedback Test Escape Analysis Test Flow Optimizations Test Generation and Validation Test Resource Partitioning **Test Standards** Testing High Speed Optics/Photonics Timing Test Yield Analysis and Optimization

